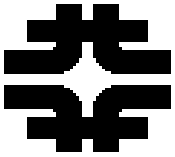

Fermilab

Particle Physics Division / CDF Upgrade Project

DRAFT

Specification for ADC/Memory Module (ADMEM)

Particle Physics Division
CDF Upgrade Project

T. Shaw

4/19/93
Revised 11/21/2001

Revision History

7/16/97	TMS	Fixed P3 Pinout Definition Fixed data shift on Flash RAM Algorithims
9/3/97	TMS	Fix typos in DAC Control Register and CAFÉ Control Register, added PLUG bit in Control Register
4/2/98	TMS	Modify Trigger Sum description
10/15/98	TMS	Update memory map, modify Trigger Sum info.
12/15/98	TMS	Update memory map
11/2/2000	TMS	Add power info
11/21/2001	TMS	Update info on “Spike Killer” trigger algorithm Pedestal Subtraction register definition revised Ped subraction moved from before linearization to after Pipeline readout function disabled

1.0 Introduction

The upgraded CDF data acquisition (DAQ) system will be capable of running at a rate of 1000 Hz into the Level 3 processing farm and will approach a "dead timeless" system. To accomplish this goal it becomes necessary to digitize the detector data at every beam crossing (132 ns).

Figure 1 presents an overview of part of the digital readout system, showing the data path from the front-end crates to the network switch into the Level 3 processing farm.

The calorimetry analog data is received by the **AD**C/**MEM**ory (ADMEM) modules. The function of the ADMEM module will be to receive the analog information (current pulses from the phototube bases), digitize it at a rate of 7.6 MHz, store the result in a pipeline, and move the data that passes Level 1 and Level 2 triggers into one of four L2 Decision buffers. The L2 Decision buffers will be accessible as slave memory through VMEbus. Figure 2 provides a functional block diagram of the module.

The ADMEM board also provides phototube tower sums to the L1 Trigger. Channel values from the ADCs will be digitally summed together across up to four channels. Pedestal subtraction will be done prior to tube summing. Sine theta weighting will be done by running the digital sum through a lookup table.

The data in the L2 Decision buffers will be read out via a VMEbus Readout Controller (VRC) and sent upstream on serial lines to VMEbus Readout Buffer (VRB) modules. These Readout Memory modules will serve to concentrate the data for readout by the SCPU over VMEbus. The SCPU will service the movement of the data onto the data switch, through which it is routed into the Level 3 processing farm.

2.0 Analog Front-end Café Modules

The Analog Front-end portion of the ADMEM board will be implemented on removable Café modules.

Each Café module will receive current pulses from a calorimetry photomultiplier tube. A current buffer will receive these pulses and drive the signal to a QIE chip. The QIE is a custom designed ASIC which integrates the charge on eight non-overlapping binary scales. The QIE outputs a two bit capacitor ID (identifying one of four internal capacitors used), a three bit exponent (identifying which of eight scales the current pulse falls in) and an analog output which is fed into a 10 bit Flash ADC.

The data resulting from the above is fed into a 1Mb Flash RAM which is used as a look-up table to linearize the results. The look-up table allows the user to subtract pedestals, adjust for offsets and gains. Table 1 shows the format of the data going into the Flash RAM look-up. Bits(14:0) come from the circuitry described above, bit 15 is a pass-through mode bit driven by the ADMEM's Control register which causes the data out to be the same as the data in.

Table 2 shows that the 16 data bits coming out of the Flash RAM look-up are interpreted as a 15 bit linearized value and a range bit which indicates a times eight factor.

The Café modules utilize 72-pin SIMM sockets. The pinout of these sockets can be seen in Table 3.

Table 4 shows the pinout of the J3 backplane connector which is used to bring in the 20 differential current pulse channels.

Flash RAM Look-up Table Address Bit	Signal Definition
0	Flash ADC bit 0
1	Flash ADC bit 1
2	Flash ADC bit 2
3	Flash ADC bit 3
4	Flash ADC bit 4
5	Flash ADC bit 5
6	Flash ADC bit 6
7	Flash ADC bit 7
8	Flash ADC bit 8
9	Flash ADC bit 9
10	QIE Exponent 0
11	QIE Exponent 1
12	QIE Exponent 2
13	QIE Capacitor ID 0
14	QIE Capacitor ID 1
15	Pass through mode bit (if set through ADMEM Control Register,data out of Flash RAM will be the same as the address into it)

Table 1. Data Format Presented at Input of the Flash RAM Look-up Table

Flash RAM Look-up Table Data Output	Signal Definition
14:0	Linear Value (14:0)
15	Range bit x8

Table 2. Data Format of Data at the Output of the Flash RAM Look-up Table

Pin Number	Signal	Pin Number	Signal
1	Digital GND	37	ADDDR(12)
2	Data(0)	38	ADDDR(13)
3	Data(1)	39	ADDDR(14)
4	Data(2)	40	EXT_CONTROL*
5	Data(3)	41	Digital VCC
6	Data(4)	42	OUT_CLK_IN
7	Data(5)	43	OUT_CLK_IN*
8	Data(6)	44	Digital GND
9	Data(7)	45	ADC_CLK_IN
10	Digital GND	46	ADC_CLK_IN*
11	Data(8)	47	Digital GND
12	Data(9)	48	RESET_IN
13	Data(10)	49	RESET_IN*
14	Data(11)	50	Digital GND
15	Data(12)	51	QIE_CLK_IN
16	Data(13)	52	QIE_CLK_IN*
17	Data(14)	53	Digital GND
18	Data(15)	54	Analog VSS (-15V)
19	Digital GND	55	Analog VEE (-5V)
20	HILO_Sel	56	Analog VCC
21	FRAM_WE*	57	Analog VCC
22	Digital GND	58	Analog VDD (+15V)
23	Digital VCC	59	Analog VDD
24	Digital VCC	60	Analog GND
25	ADDDR(0)	61	VCAL-
26	ADDDR(1)	62	VCAL+
27	ADDDR(2)	63	Analog GND
28	ADDDR(3)	64	CAL_EN
29	ADDDR(4)	65	CUR_AMP_EN
30	ADDDR(5)	66	PATH_SELECT
31	ADDDR(6)	67	Analog GND
32	ADDDR(7)	68	Analog GND
33	ADDDR(8)	69	Analog GND
34	ADDDR(9)	70	SIG_RET
35	ADDDR(10)	71	SIG_IN
36	ADDDR(11)	72	Analog GND

Table 3. Pinout of the Café Module

Pin Number	Row z	Row A	Row B	Row C	Row d
1	AGND	QIE_RESET	QIE_CLOCK	OUT_CLOCK	AGND
2	AGND	AGND	ADC_CLOCK	AGND	AGND
3	AGND	AGND	AGND	AGND	AGND
4	AGND	AGND	AGND	AGND	AGND
5	AGND	AGND	AGND	AGND	AGND
6	AGND	AGND	AGND	AGND	AGND
7	AGND	AGND	AGND	AGND	AGND
8	AGND	AGND	AGND	AGND	AGND
9	AGND	AGND	AGND	AGND	AGND
10	AGND	AGND	AGND	AGND	AGND
11	AGND	AGND	AGND	AGND	AGND
12	AGND	AGND	AGND	SIGNAL_IN(0)	AGND
13	AGND	SIGNAL_IN(1)	AGND	AGND	AGND
14	AGND	AGND	AGND	SIGNAL_IN(2)	AGND
15	AGND	SIGNAL_IN(3)	AGND	AGND	AGND
16	AGND	AGND	AGND	SIGNAL_IN(4)	AGND
17	AGND	SIGNAL_IN(5)	AGND	AGND	AGND
18	AGND	AGND	AGND	SIGNAL_IN(6)	AGND
19	AGND	SIGNAL_IN(7)	AGND	AGND	AGND
20	AGND	AGND	AGND	SIGNAL_IN(8)	AGND
21	AGND	SIGNAL_IN(9)	AGND	AGND	AGND
22	AGND	AGND	AGND	SIGNAL_IN(10)	AGND
23	AGND	SIGNAL_IN(11)	AGND	AGND	AGND
24	AGND	AGND	AGND	SIGNAL_IN(12)	AGND
25	AGND	SIGNAL_IN(13)	AGND	AGND	AGND
26	AGND	AGND	AGND	SIGNAL_IN(14)	AGND
27	AGND	SIGNAL_IN(15)	AGND	AGND	AGND
28	AGND	AGND	AGND	SIGNAL_IN(16)	AGND
29	AGND	SIGNAL_IN(17)	AGND	AGND	AGND
30	AGND	AGND	AGND	SIGNAL_IN(18)	AGND
31	AGND	SIGNAL_IN(19)	AGND	AGND	AGND
32	AGND	AGND	AGND	AGND	AGND

Table 4. Signal Definition of J3 Connector

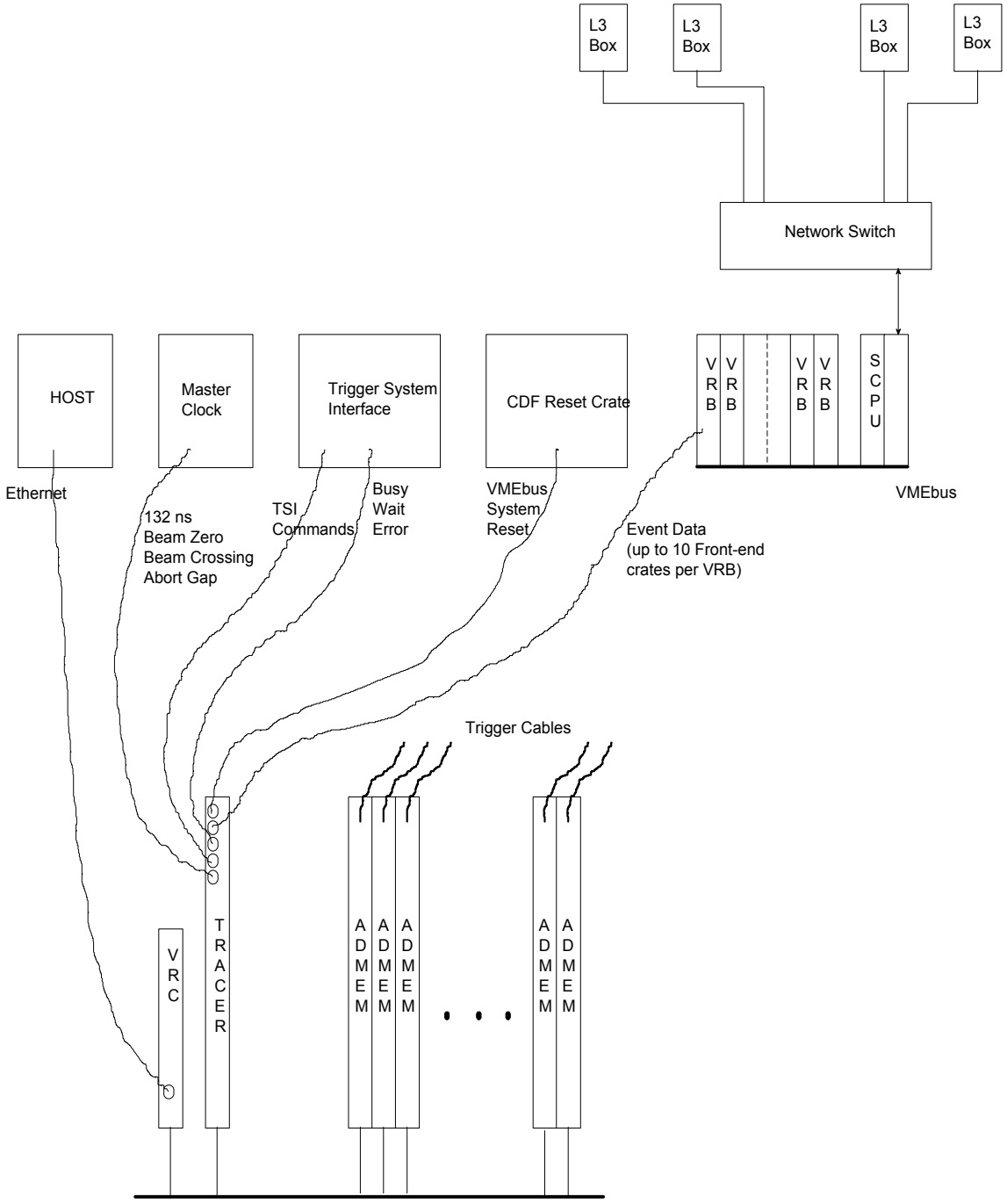

Figure 1. Digital Data Path Overview

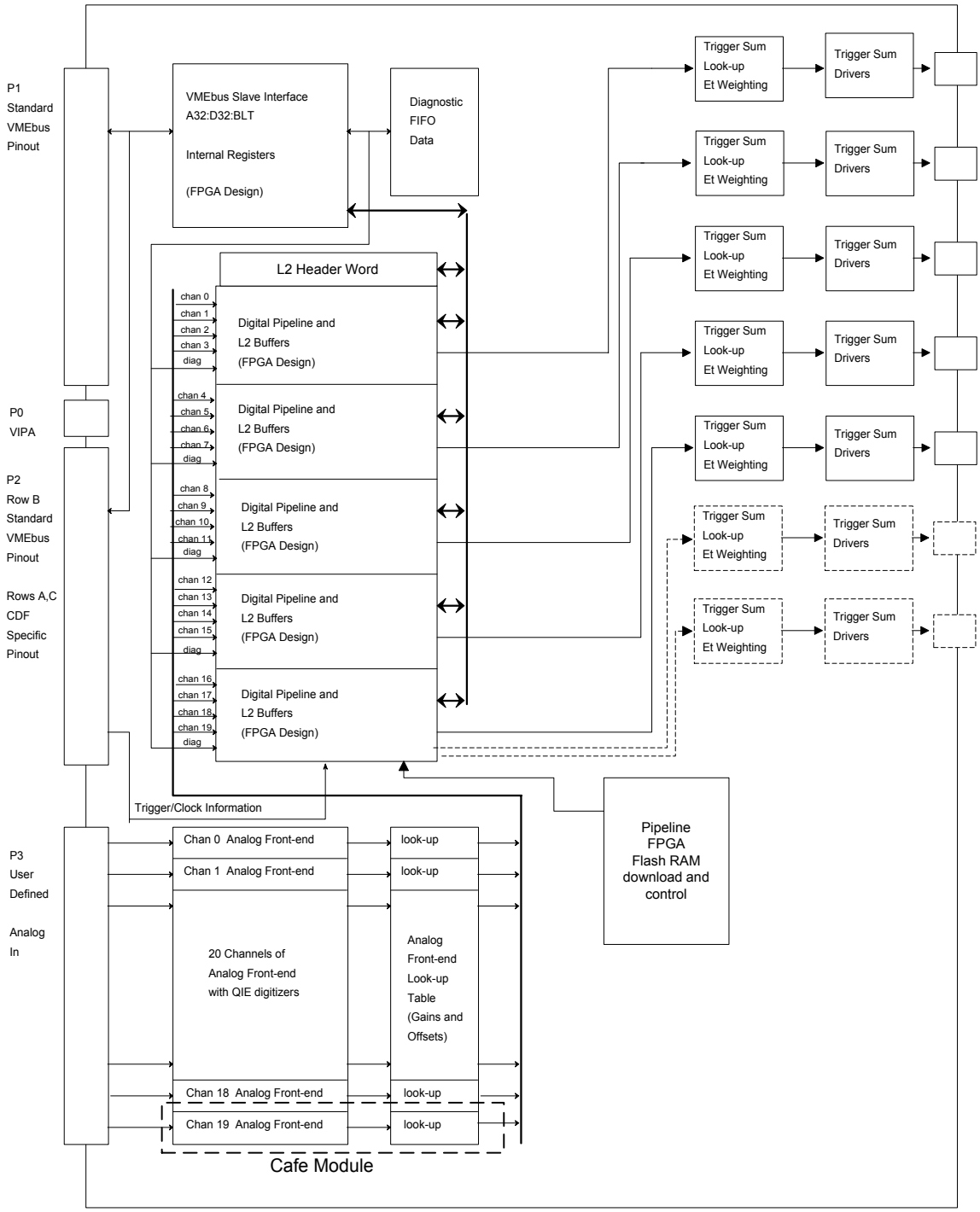

Figure 2. Block Diagram of FE/ADC/Memory Module

3.0 Look-up Table Memory

The result of the ADC conversion will be run through a memory look-up table that will be preloaded to take out desired range and offset information. The 16-bit data will then be loaded into the digital storage pipeline.

It is also possible to set a pass-through mode on the lookup memories, so that one is able to send the raw data through the memory. This is done by setting the "Enable Pass through mode on QIE data lookup tables" bit (30) of the ADMEM's Control register. **Note that this assumes the upper half of the memory has been filled with sequential data matching the lower 16 address bits.**

The Flash RAM device being used for this look-up function is AMD's AM29F100B-75EC. Like all Flash RAM, a specific algorithm must be used when erasing or programming the contents. In addition, certain ADMEM control bits and registers must be set correctly in order for the contents to be changed.

Two examples below describe how to set up the erase and the write algorithms to these devices. For additional information on these devices, please refer to AMD's data sheet.

To erase the Flash RAM

- set the "Enable VMEbus access to Flash RAM data lookup tables" bit (29) of the ADMEM's Control register
- write the correct value to the ADMEM's Access Register for Flash RAM. Currently this value has been set to 0xBEAD0000
- Select which bank of Flash RAM you wish to address by writing to the Flash RAM Select Register
- Now write the erase algorithm to the Flash RAM Data register

```
write 0xAA 0000   to    addr  0xYY51 5554  (YY is Geo. Address)
write 0x55 0000   to          0xYY50 AAA8
write 0x80 0000   to          0xYY51 5554
write 0xAA 0000   to          0xYY51 5554
write 0x55 0000   to          0xYY50 AAA8
write 0x10 0000   to          0xYY51 5554
```

To write the Flash RAM

- set the "Enable VMEbus access to Flash RAM data lookup tables" bit (29) of the ADMEM's Control register
- write the correct value to the ADMEM's Access Register for Flash RAM. Currently this value has been set to 0xBEAD0000
- Select which bank of Flash RAM you wish to address by writing to the Flash RAM Select Register
- Now write the program algorithm to the Flash RAM Data register

```
write 0xAA 0000          to    addr  0xYY51 5554
write 0x55 0000          to          0xYY50 AAA8
write 0xA0 0000          to          0xYY51 5554
write desired data       to    desired adrress
```

4.0 Digital Pipeline and L2 Buffers

The ADCs on the ADMEM module are required to digitize analog detector information every beam crossing (132 ns). This digitized data must be stored in a digital pipeline for a maximum period of 4+ us or 42 crossings. This is the period of time it takes the Level 1 trigger decision to reach the front-end crates. A Level 1 Accept causes the data to be written into one of four L2 Decision buffers, based upon the buffer address supplied by the Trigger System Interface (TSI). A Level 1 Reject will cause the data at the end of the storage pipeline to be lost.

The TSI will keep track of all Level 2 Decision buffer status. Buffers will be overwritten with new Level 1 Accept data if a Level 2 Reject has occurred on a given buffered event.

A Level 2 Accept will cause the VMEbus Readout Controller (VRC) to address each ADMEM card within the crate and do a block read of all channel data for a particular buffer address.

The digital pipeline and Level 2 buffers will be implemented with Xilinx FPGAs, see Figure 3. Currently, Xilinx's XC4013EPQ240-3 FPGA is the targeted device. The FPGA design takes in four channels worth of data from the Café Modules.

A separate diagnostic path allows the user to send a pre-determined set of diagnostic data through the pipeline chip. The diagnostic data can be directed through a single channel or a mask set of channels and comes from the Diagnostic FIFO shown in the ADMEM block diagram (Fig. 2). The FIFO data is 8k deep and will loop back on itself when the FIFO empties.

A multiplexing stage allows the user to select between the diagnostic data path or the default Café module data. At the output of the multiplex stage, data is moved into both the pipeline stage (implemented as a circular buffer) and the Trigger Sum logic.

Trigger Sums are formed by adding up to four channels worth of data. The Trigger Sum data is then sent out of the FPGA, to the Trigger Sum look-up tables.

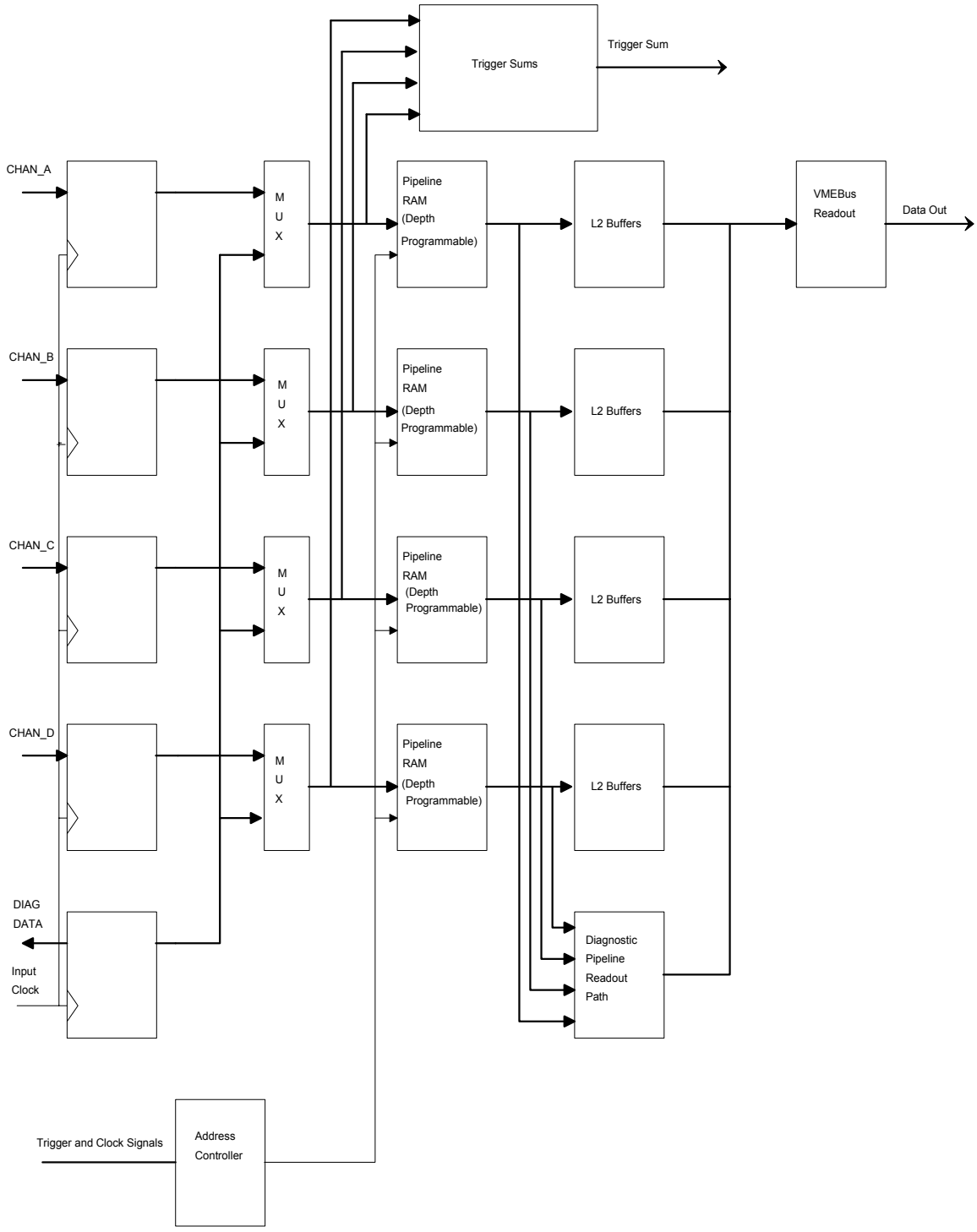

Figure 3. Block Diagram of the ADMEM's Digital Pipeline

The pipeline is of programmable depth; however, it has a maximum limit of 64 stages. The depth of the pipeline should be set to 42 stages minus the number of stages taken up in the analog section. At the output of the pipeline stage, a L1 Accept will cause the data to be stored into one of four L2 Decision Buffers. A L1 Reject causes the data to be lost. L2 Decision buffers are available for readout over VMEbus.

Below feature disabled Nov/2001 in order to free up space in FPGA

A path is also provided to allow the user to read out the Pipeline RAM after the system has been put into a "halt" condition" and the "Enable VMEbus read of Pipeline Data" bit has been set in the Control Register.

5.0 Trigger Interface

The communication with the Trigger System Interface (TSI) requires the passing of several protocol signals between it and the front end crates. At the front end crate, all signals passing between it and the TSI will be handled by the **TR**igger **A**nd **C**lock + **E**vent **R**eadout Module (TRACER) located in Slot 2 of the VMEbus crate.

The TRACER will receive signals from the Trigger supervisor, digitally process them and then fan them out to the ADMEM modules over the J2 backplane. CDF Note 2388 defines the exact pinout of the custom J2 backplane and the custom signals it routes.

6.0 Trigger Sums

ADMEM boards must provide phototube channel sums to the Trigger. Channel values from up to 4 channels will summed together digitally. The pipeline chip will provide up to 15 trigger sum bits. The bits will the be fed into the lookup memories where they are mapped into 10 output bits. Et weighting will be done through the lookup memories. It is possible to bypass Et weighting by setting a pass-through bit, "Enable Pass through mode on Trigger Sum data", in the Control Register.

The devices used for the Trigger Sum look up tables are identical to those used by the Café Modules, and examples of erase and write algorithms apply.

- To form a trigger sum, the following logic is followed:
- Read in the 16 bits of data coming from the Café module.
- If the MSB is set, multiply the number by 8 - all numbers are now 18 bits.
- Subtract an 7 bit pedestal (programmed by user).
- Add 1, 2, or 4 (depending on the type of trigger sum) of these numbers together to get the raw Trigger Sum.
- Produce a 15 bit Trigger Sum which will be presented to the Look-up Table.
    - In the case of a 1 Tube "Sum", truncate the 18 bit sum by dropping the 3 least significant bits.
    - In the case of a 2 Tube Sum, truncate the 19 bit sum by dropping the 4 least significant bits.
    - In the case of a 4 Tube Sum, truncate the 20 bit sum by dropping the 2 least significant bits and the 3 most significant bits. Additionally, if any of the three most significant bits are set, saturate the output by setting all 15 output bits to "1".

      The 4 tube sum used in the central calorimeter now also incorporates the use of a "Spike Killer" bit which can be turned on by writing to the Pedestal Subration registers. If the "Spike Killer" bit is set, a single tube "spike" will be zeroed out by the hardware when an adjacent tube is below a given pedestal.

      Please refer to CDF/DOC/TRIGGER/PUBLIC/4781 "Specification for the Trigger Tower Summing and E_T Weighting for ADMEM Boards"
- Present the 15 bit Trigger Sum to the Flash RAM Look-up Table.
- Data which has been sine theta weighted comes out of the Trigger Sum Look-up Tables (assumes appropriate mapping values have been pre-loaded) and is registered.
- The sums will be transmitted to the trigger system on parallel copper cable, using LVDS drivers, through connectors on the front panel at a rate of one sum per crossing (where a crossing is assumed to be 132 ns).

Table 5 illustrates the mapping between the derived 15-bit Raw Trigger Sum (the one prior to going through the Look-up Table) and the look-up table address bits.

Flash RAM Look-up Table Address Bit	Signal Definition
0	Raw Trigger Sum (0)
1	Raw Trigger Sum (1)
2	Raw Trigger Sum (2)
3	Raw Trigger Sum (3)
4	Raw Trigger Sum (4)
5	Raw Trigger Sum (5)
6	Raw Trigger Sum (6)
7	Raw Trigger Sum (7)
8	Raw Trigger Sum (8)
9	Raw Trigger Sum (9)
10	Raw Trigger Sum (10)
11	Raw Trigger Sum (11)
12	Raw Trigger Sum (12)
13	Raw Trigger Sum (13)
14	MSB Trigger Sum (14)
15	Pass through mode bit

Table 5. Data Format of Data at the Output of the Flash RAM Look-up Table

Table 6 illustrates the pinout of the 20-pin SCSI II (FCN-235D020-G/E) connector chosen for use.

Pin number	Signal	Pin Number	Signal
1	sum(0)	2	sum(0)*
3	sum(1)	4	sum(1)*
5	sum(2)	6	sum(2)*
7	sum(3)	8	sum(3)*
9	sum(4)	10	sum(4)*
11	sum(5)	12	sum(5)*
13	sum(6)	14	sum(6)*
15	sum(7)	16	sum(7)*
17	sum(8)	18	sum(8)*
19	sum(9)	20	sum(9)*

Table 6. Pinout Definition of Trigger Sum connectors

Figure 4 provides a simplified drawing of the ADMEM's Front Panel, and shows which connector corresponds to which trigger sum. As can be seen, there is a difference in how Trigger Sums are formed and output, depending on whether the board is to be used in the Central or Plug Calorimetry. These differences are made by downloading different configuration patterns to the FPGA which handles channels 16, 17, 18 and 19.

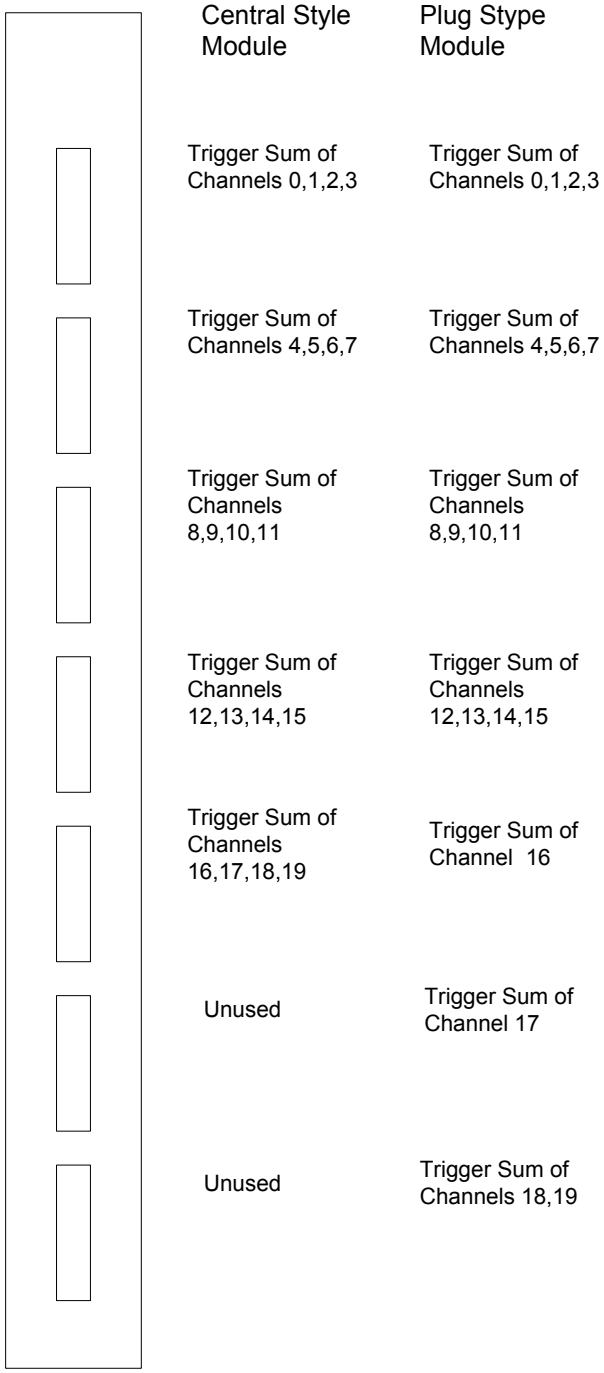

Figure 4. Simple Front Panel View of Trigger Sum Ports

7.0 L2 Header Word

The L2 Header word is the first word which is to be read out of a L2 buffer Space. The purpose and description of this word can be found in CDF3145 - Specification of DAQ/Trigger Synchronization Checking Protocol and VME board Header word.

Following the specification of CDF3145, the ADMEM board provides a the following header word at the beginning of the four VMEbus L2 Buffer spaces:

L2 Buffer 0 Header Word **(R)**

Bit	**Function**
0-7	Bunch ID: 8 bit counter from Bunch Zero
8-12	Geographical Address
13-22	Board Serial Number
23-31	Board Type

The Bunch ID has an associated offset, which is set through the ADMEM's Pipeline Offset Register. The Geographical Address comes from the VMEbus backplane pins and the Board Serial Number and Board Type are programmed on hardwired switches.

8.0 Diagnostic Channel Data

As previously mentioned, there is a Diagnostic FIFO which allows the user to download a pattern of data which can then be pumped through the L1 Pipeline and Trigger Sum logic in place of the Café module data.

In order to do this,

- write to the Diagnostic Pipeline Data FIFO,
- select the Channels for which the diagnostic data will be used by writing to the Pipeline Diagnostic Channels Enable Register,
- and set the "Enable Diagnostic Pipeline Data" bit in the Control register.

The Diagnostic FIFO will begin pumping out data on the first Beam_Zero marker following a CDF Halt-Recover-Run sequence. When the FIFO empties, it will begin to re-transmit, ensuring a constant flow of diagnostic data.

9.0 FPGA Download

The Pipeline FPGAs, L2 Header FPGA, and the CAFÉ Timing FPGA on the ADMEM board are downloaded from Flash RAM.

To download the board from Flash RAM, the configuration bitstream must be downloaded to the Pipeline Download Flash RAM. Unlike the other Flash RAMs onboard, this one is operated in 8 bit mode rather than 16 bit mode, so programming and erase algorithms differ.

The Pipeline Flash RAM is downloaded any time the board is plugged in, or whenever the "Program Pipeline" bit of the Control Register is toggled high-low.

10.0 VME Slave Interface

The ADMEM will implement a modified version of a VMEbus slave interface. Only 32 bit aligned data transfers will be supported; these may be either single word transfers or block transfers. Only extended (32-bit) addressing modes will be supported. All boards will be assigned a unique geographical address through use of backplane pins on the VIPA J1 backplane. ADMEM modules will respond to the following address modifier codes: 09, and 0B.

Memory Map

YYY0 0000 Diagnostic Register (32 bits) **(R/W)**

YYY0 0004 Control

Bit	Function
31	Software Reset (clears the Diagnostic FIFO) **(R/W)**
30	Enable Pass through mode on QIE data lookup tables **(R/W)** Lookup table will utilize upper half of 1Mb range
29	Enable VMEbus access to Flash RAM data lookup tables **(R/W)** VMEbus write control over Flash RAM will be allowed
28	Enable VMEbus read of Pipeline data **(R/W)**
27	Enable Diagnostic Pipeline Data **(R/W)** Data from Diagnostic FIFO, rather than Analog Café modules, will be used for channels indicated in the Pipeline Diagnostic Channels Enable Register
26	Enable Pass through mode on Trigger Sum data **(R/W)** Lookup table will utilize upper half of 1Mb range
25	Program Pipeline **(R/W)**
24	Undefined
23	Diagnostic FIFO E/F* **(R)**
22	Diagnostic FIFO H/F* **(R)**
21	Diagnostic FIFO PAFE* **(R)**
20	Undefined
19	Undefined
18	Undefined
17	Plug Calorimetry Configuration **(R)**
16	Pipeline FPGA Download Done **(R)**

YYY0 0008 Access Register for Flash RAM **(R/W)**
(must be set to 0xBEAD0000 in order to write to Flash RAM)

Bit	Function
31-16	Enable VMEbus write to FRAM code (15:0)

YY00 000C Pipeline Length **(R/W)**
Description: Depth of pipeline should programmed to be 42 minus the number of stages in analog circuitry.

Bit	Function
24-31	Programmable pipeline depth

YY00 0010 Pipeline Offset **(R/W)**
Description: Offset should be programmed to equal #stages in analog circuitry.

Bit	Function
24-31	Programmable pipeline depth

YY00 0014 Flash Ram Select **(R/W)**

Description: Selects which channel of FRAM is being addressed over VMEbus.

Bit	**Function**
31	Undefined
30	Undefined
29	Undefined
28	Select Flash RAM Channel(4)
27	Select Flash RAM Channel(3)
26	Select Flash RAM Channel(2)
25	Select Flash RAM Channel(1)
24	Select Flash RAM Channel(0)
23-0	Undefined

Channel 0-19 map to Café Modules 0-19
Channel 20-26 map to trigger sum lookup table (0-6)
Channel 27 maps to Pipeline FPGA Download

YY00 0018 Pipeline Diagnostic Channels Enable Register **(R/W)**

Description: Selects channels through which diagnostic data from the Diagnostic Pipeline FIFO will be pumped. This register will act as a mask to select channels through which the diagnostic data will flow. This register is effective only when the "Enable Diagnostic Pipeline Data" bit in the Control Register has been set.

Bit	**Function**
31-20	Undefined
19	Selects Channel 19
18	Selects Channel 18
17	Selects Channel 17
16	Selects Channel 16
15	Selects Channel 15
14	Selects Channel 14
13	Selects Channel 13
12	Selects Channel 12
11	Selects Channel 11
10	Selects Channel 10
9	Selects Channel 9
8	Selects Channel 8
7	Selects Channel 7
6	Selects Channel 6
5	Selects Channel 5
4	Selects Channel 4
3	Selects Channel 3
2	Selects Channel 2
1	Selects Channel 1
0	Selects Channel 0

YY00 001C DAC Data Register **(R/W)**

Description: This register drives the Data inputs of the Calibration DAC (Analog Device's AD760)

Bit	**Function**
0-7	DAC Data

YY00 0020 DAC Control Register **(R/W)**

Description: This register drives the Control inputs of the Calibration DAC (Analog Device's AD760)

Bit	**Function**
0	Chip_select
1	Low Byte Enable
2	High Byte Enable
3	Clear
4	Load DAC
5	Calibrate

YY00 0024 DAC Status Register **(R)**

Description: This register allows the readout of the CALOK signal which comes from the Calibration DAC (Analog Device's AD760)

Bit	**Function**
0	DAC Calibrate OK

YY00 0028 Café Control Register **(R/W)**

Description: This register provides control over the Café module calibration.

Bit	**Function**
0	Café Calibrate Enable 1
1	Café Calibrate Enable 2
2	Café Calibrate Enable 3
3	Café Calibrate Enable 4
4	Café SMON Enable
5	Café Path Select

YY00 002C Café Delay Register **(R/W)**

Description: This register delays phase of the CDF_CLOCK signal to the Café module conversion logic. 1 Count represents 1 ns.

Bit	**Function**
0-7	Delay Value

YY00 0030 Transition Port Register **(R/W)**

Description: This register allows 16 data lines to be driven to the transition module.

Bit	**Function**
16-31	Data Value

YY00 0034 Channels (0-3) Trigger Sum Subtraction pedestal Register **(R/W)**
Description: This register represents the value subtracted from the Café module data prior to summing.

Bit	**Function**
31	Spike Killer Enable
24-30	Pedestal Value

YY00 0038 Channels (3-7) Trigger Sum Subtraction pedestal Register **(R/W)**
Description: This register represents the value subtracted from the Café module data prior to summing.

Bit	**Function**
31	Spike Killer Enable
24-30	Pedestal Value

YY00 003C Channels (8-11) Trigger Sum Subtraction pedestal Register **(R/W)**
Description: This register represents the value subtracted from the Café module data prior to summing.

Bit	**Function**
31	Spike Killer Enable
24-30	Pedestal Value

YY00 0040 Channels (12-15) Trigger Sum Subtraction pedestal Register **(R/W)**
Description: This register represents the value subtracted from the Café module data prior to summing.

Bit	**Function**
31	Spike Killer Enable
24-30	Pedestal Value

YY00 0044 Channels (16-19) Trigger Sum Subtraction pedestal Register **(R/W)**
Description: This register represents the value subtracted from the Café module data prior to summing.

Bit	**Function**
31	Spike Killer Enable
24-30	Pedestal Value

YY10 0000 - YY10 007F ID PROM (upper 8 bits) **(R)**

This function was disable Nov/2001 in order to free space in the FPGAs

NOTE: Digital Pipeline is READ only, each read will advance the Pipeline Address for the addressed FPGA by one. The Enable Pipeline Read bit must be set in the control register. A Pipeline Read should only be done after a HALT condition has been set.

YY40 0000 - YY40 0XXX	Pipeline Contents channel 0 **(R)**
YY40 1000 - YY40 1XXX	Pipeline Contents channel 1 **(R)**
YY40 2000 - YY40 2XXX	Pipeline Contents channel 2 **(R)**
YY40 3000 - YY40 3XXX	Pipeline Contents channel 3 **(R)**
YY40 4000 - YY40 4XXX	Pipeline Contents channel 4 **(R)**
YY40 5000 - YY40 5XXX	Pipeline Contents channel 5 **(R)**
YY40 6000 - YY40 6XXX	Pipeline Contents channel 6 **(R)**
YY40 7000 - YY40 7XXX	Pipeline Contents channel 7 **(R)**
YY40 8000 - YY40 8XXX	Pipeline Contents channel 8 **(R)**
YY40 9000 - YY40 9XXX	Pipeline Contents channel 9 **(R)**
YY40 A000 - YY40 AXXX	Pipeline Contents channel 10 **(R)**
YY40 B000 - YY40 BXXX	Pipeline Contents channel 11 **(R)**
YY40 C000 - YY40 CXXX	Pipeline Contents channel 12 **(R)**
YY40 D000 - YY40 DXXX	Pipeline Contents channel 13 **(R)**
YY40 E000 - YY40 EXXX	Pipeline Contents channel 14 **(R)**
YY40 F000 - YY40 FXXX	Pipeline Contents channel 15 **(R)**
YY41 0000 - YY41 0XXX	Pipeline Contents channel 16 **(R)**
YY41 1000 - YY41 1XXX	Pipeline Contents channel 17 **(R)**
YY41 2000 - YY41 2XXX	Pipeline Contents channel 18 **(R)**
YY41 3000 - YY41 3XXX	Pipeline Contents channel 19 **(R)**

YY50 0000 - YY5C FFFC Flash RAM Data Register **(R/W)**
If the FLASH RAM Select Register is set to 0 thru 1A(hex)
Bits 31:16 are used
If the FLASH RAM Select Register is set to 1B(hex)
Bits 31:24 are used
(Read/Write only when enables set in control register)

YY60 0000 - YY6X XXXX Diagnostic Pipeline Data FIFO **(R/W)**

NOTE: All L2 Buffers are Read Only

YY80 0000 L2 Buffer 0 Header Word **(R)**

Bit	Function
0-7	Bunch ID: 8 bit counter from Bunch Zero
8-12	Geographical Address
13-22	Board Serial Number
23-31	Board Type

YY80 0004 Channel 0,1 L2 Buffer 0 **(R)**
YY80 0008 Channel 2,3 L2 Buffer 0 **(R)**
YY80 000C Channel 4,5 L2 Buffer 0 **(R)**
YY80 0010 Channel 6,7 L2 Buffer 0 **(R)**
YY80 0014 Channel 8,9 L2 Buffer 0 **(R)**
YY80 0018 Channel 10,11 L2 Buffer 0 **(R)**
YY80 001C Channel 12,13 L2 Buffer 0 **(R)**
YY80 0020 Channel 14,15 L2 Buffer 0 **(R)**
YY80 0024 Channel 16,17 L2 Buffer 0 **(R)**
YY80 0028 Channel 18,19 L2 Buffer 0 **(R)**

YY90 0000 L2 Buffer 1 Header Word **(R)**

Bit	Function
0-7	Bunch ID: 8 bit counter from Bunch Zero
8-12	Geographical Address
13-22	Board Serial Number
23-31	Board Type

YY90 0004 Channel 0,1 L2 Buffer 1 **(R)**
YY90 0008 Channel 2,3 L2 Buffer 1 **(R)**
YY90 000C Channel 4,5 L2 Buffer 1 **(R)**
YY90 0010 Channel 6,7 L2 Buffer 1 **(R)**
YY90 0014 Channel 8,9 L2 Buffer 1 **(R)**
YY90 0018 Channel 10,11 L2 Buffer 1 **(R)**
YY90 001C Channel 12,13 L2 Buffer 1 **(R)**
YY90 0020 Channel 14,15 L2 Buffer 1 **(R)**
YY90 0024 Channel 16,17 L2 Buffer 1 **(R)**
YY90 0028 Channel 18,19 L2 Buffer 1 **(R)**

YYA0 0000 L2 Buffer 2 Header Word **(R)**

Bit	Function
0-7	Bunch ID: 8 bit counter from Bunch Zero
8-12	Geographical Address
13-22	Board Serial Number
23-31	Board Type

YYA0 000C Channel 4,5 L2 Buffer 2 **(R)**
YYA0 0010 Channel 6,7 L2 Buffer 2 **(R)**
YYA0 0014 Channel 8,9 L2 Buffer 2 **(R)**
YYA0 0018 Channel 10,11 L2 Buffer 2 **(R)**
YYA0 001C Channel 12,13 L2 Buffer 2 **(R)**
YYA0 0020 Channel 14,15 L2 Buffer 2 **(R)**
YYA0 0024 Channel 16,17 L2 Buffer 2 **(R)**
YYA0 0028 Channel 18,19 L2 Buffer 2 **(R)**

YYB0 0000 L2 Buffer 3 Header Word **(R)**

Bit	Function
0-7	Bunch ID: 8 bit counter from Bunch Zero
8-12	Geographical Address
13-22	Board Serial Number
23-31	Board Type

YYB0 0004 Channel 0,1 L2 Buffer 3 **(R)**
YYB0 0008 Channel 2,3 L2 Buffer 3 **(R)**
YYB0 000C Channel 4,5 L2 Buffer 3 **(R)**
YYB0 0010 Channel 6,7 L2 Buffer 3 **(R)**
YYB0 0014 Channel 8,9 L2 Buffer 3 **(R)**
YYB0 0018 Channel 10,11 L2 Buffer 3 **(R)**
YYB0 001C Channel 12,13 L2 Buffer 3 **(R)**
YYB0 0020 Channel 14,15 L2 Buffer 3 **(R)**
YYB0 0024 Channel 16,17 L2 Buffer 3 **(R)**
YYB0 0028 Channel 18,19 L2 Buffer 3 **(R)**

YY is the VME geographical address of the ADMEM.

11.0 ADMEM Power Requirements

Digital Sections:

VPC 0 A

VCC 2.815 A

Analog Sections:

+5 910 ma

-5 25 ma

+15 1.625 A

-15 305 ma